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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/536,646	03/28/00	KATSURA	K 500.26967RC1

020457
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EXAMINER	
CHAUHAN, U	
ART UNIT	PAPER NUMBER
2671	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/536,646	Applicant(s) KATSURA ET AL.	
	Examiner Ulka J. Chauhan	Art Unit 2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *07/302,332* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Reissue Applications

1. The parent reissue application 07/985,141 issued without any cross reference to the continuation reissue application 09/536,646; amendment of the parent reissue patent RE37103, to include a cross-reference to the continuation is required by a Certificate of Correction.

2. Applicant is reminded of the continuing obligation under 37 CFR 1.56 to timely apprise the Office of any litigation information, or other prior or concurrent proceeding, involving Patent No. 4,975,857, which is material to patentability of the claims under consideration in this reissue application. This obligation rests with each individual associated with the filing and prosecution of this application for reissue. See MPEP §§ 1404, 1442.01 and 1442.04.

3. The reissue oath/declaration filed with this application is defective (see 37 CFR 1.175 and MPEP § 1414) because of the following: the error identified in the declaration, based upon which this application is filed, is identical to the error identified for the parent reissue application 07/985,141. This error was fixed as the parent reissue application 07/985,141 issued as US RE37,103 E.

4. Claims 1-46 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175. The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

5. In accordance with 37 CFR 1.175(b)(1), a supplemental reissue oath/declaration under 37 CFR 1.175(b)(1) must be received before this reissue application can be allowed.

6. Receipt of an appropriate supplemental oath/declaration under 37 CFR 1.175(b)(1) will overcome this rejection under 35 U.S.C. 251. An example of acceptable language to be used in the supplemental oath/declaration is as follows:

> "Every error in the patent which was corrected in the present reissue application, and is not covered by a prior oath/declaration submitted in this application, arose without any deceptive intention on the part of the applicant."

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

8. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

9. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 9, 14, 24, 28, and 33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. RE37,103 E in view of U.S. Patent No. 4,750,154 to Lefsky et al. Although the conflicting claims are not identical, they are not patentably distinct from each other. The elements recited in claims 9, 24, 28, and 33 are all claimed in claim 14 of U.S. Patent No. RE37,103 E except "a storage which temporarily stores graphics data read out from said memory". This is what Lefsky teaches. Lefsky discloses a write buffer 16 disposed between a processor and a memory for storing data to be transferred between the processor and the memory at Fig. 1. Lefsky discloses that providing a write buffer reduces the performance costs associated with the transfer of data

between the processor and the memory at col. 1 lines 24-30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of U.S. Patent No. RE37,103 E and Lefsky such that a write buffer ("a storage which temporarily stores graphics data read out from said memory") is provided in the memory controller of U.S. Patent No. RE37,103 E so that the performance costs of transferring data from the memory to the processor are reduced.

11. With respect to claim 14 of the instant application, all of the elements are recited in claim 14 of U.S. Patent No. RE37,103 E except a DAC which outputs graphics data read from memory and "a storage which temporarily stores graphic data read out from said memory". Official Notice is taken that both the concept and advantage of DAC are well known and expected in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a DAC for outputting data read from memory in the proper format for display on a monitor. Further, Lefsky discloses a write buffer 16 disposed between a processor and a memory for storing data to be transferred between the processor and the memory at Fig. 1. Lefsky discloses that providing a write buffer reduces the performance costs associated with the transfer of data between the processor and the memory at col. 1 lines 24-30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of U.S. Patent No. RE37,103 E and Lefsky such that a write buffer ("a storage which temporarily stores graphics data read out from said memory") is provided in the memory controller of U.S. Patent No. RE37,103 E so that the performance costs of transferring data from the memory to the processor are reduced.

12. Claim 43 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 9 of U.S. Patent No. RE37,103 E in view of U.S. Patent No. 4,750,154 to Lefsky et al. Although the conflicting claims are not identical, they are not patentably distinct from each other. The elements recited in claim 43 are all claimed in claim 9 of U.S. Patent No. RE37,103 E except "a storage which temporarily stores graphics data read out from said memory". This is what Lefsky teaches. Lefsky discloses a write buffer 16 disposed between a processor and a memory for storing data to be transferred between the processor and the memory at Fig. 1. Lefsky discloses that providing a write buffer reduces the performance costs associated with the transfer of data between the processor and the memory at col. 1 lines 24-30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of U.S. Patent No. RE37,103 E and Lefsky such that a write buffer ("a storage which temporarily stores graphics data read out from said memory") is provided in the memory controller of U.S. Patent No. RE37,103 E so that the performance costs of transferring data from the memory to the processor are reduced.

13. Claims 22 and 41 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. RE37,103 E in view of U.S. Patent No. 4,639,890 to Heilveil et al. Although the conflicting claims are not identical, they are not patentably distinct from each other. The elements recited in claims 22 and 41 are all claimed in claim 14 of U.S. Patent No. RE37,103 E except "a digital to analog converter" for claim 22 and "a first circuit which reads out a plurality of graphic data at different column addresses at a same row address from said memory" for both claims 22 and 41. Official Notice is taken that both the concept and advantage of DAC are well known and expected in the art.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a DAC for outputting data read from memory in the proper format for display on a monitor. Further, Heilveil teaches a video display system in which the memory 5 includes a storage array 10 composed of rows and columns of memory cells at col. 4 lines 58-62 where the memory is operated in page mode format in which the row address is kept the same and successive column addresses are strobed onto the chip such that the memory access time is reduced at col. 9 lines 10-20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of U.S. Patent No. RE37,103 E and Heilveil such that the memory of U.S. Patent No. RE37,103 E is implemented to be operable in a page mode format to reduce memory access times.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

15. Claims 4-7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 4,823,286 to Lumelsky et al.

16. As per claim 4, Lumelsky discloses a system including memory means (20), data processing means (18) and output means (output from memory 20 to a monitor) in Fig. 1. The memory control means is disclosed in Figs. 8-11 and 15-17.

17. As per claim 5, Lumelsky discloses pixels including plural bits at Fig. 2.

18. As per claim 6, Lumelsky discloses a system that allows for the selection of the number of bits accessed for each pixel (Figs. 3-7 show accessing 8, 4, or 1 bit per pixel).

19. As per claim 7, Lumelsky discloses that a register is provided to temporarily store the data at col. 10 lines 61-66.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

22. Claims 1-3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,823,286 to Lumelsky et al and U.S. Patent No. 5,113,369 to Kinoshita.

23. As per claims 1-3 and 8, Lumelsky discloses a system including memory means (20), data processing means (18) and output means (output from memory 20 to a monitor) in Fig. 1. The memory control means is disclosed in Figs. 8-11 and 15-17. Lumelsky does not expressly teach memory control means that connect an n-bit data bus and an m-bit data bus. Kinoshita

discloses this at col. 3 line 40-col. 4 line 49, col. 5 lines 10-51, claim 7, and Figs. 2 and 3. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Lumelsky and Kinoshita such that the data accessed from memory over a 16-bit bus can be easily used by a 32-bit processor.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art teach various graphics display systems.

U.S. Patent No. 4237543 to Nishio et al. U.S. Patent No. 4326202 to Kidode et al.

U.S. Patent No. 4839801 to Nicely et al. 4866603 to Chiba

U.S. Patent No. 4943937 to Kasano et al. U.S. Patent No. 4959771 to Ardini, Jr. et al.

U.S. Patent No. 5027290 to Kirk et al. U.S. Patent No. 5057837 to Colwell et al.

U.S. Patent No. 5185599 to Doornink et al.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ulka Chauhan** whose telephone number is **(703) 305-9651**. The examiner can normally be reached Mon.-Fri. from 9:00 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Mark Zimmerman**, can be reached at **(703) 305-9798**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

26. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-4700.

Ulka J. Chauhan
Primary Examiner
Art Unit 2671

ujc
October 21, 2001